# Design Examples of On Board Dual Supply Voltage Logic Translators

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## Introduction

Logic translators can be used to connect ICs together that are located on the same PCB and use different supply voltages. Figure 1 lists popular applications that use dual supply voltage translators to interface a microprocessor and peripheral IC. The following design examples will be discussed in this document:

- $I^2C^{TM}$  Bus
  - SMBus
  - PMBus
- SPI Bus
- Memory Mapped I/O
- UARTs
- USB Ports



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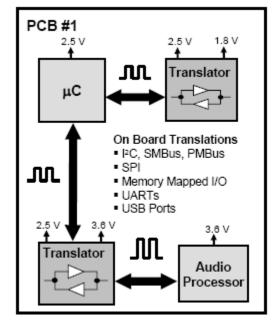


Figure 1. Dual Power Supply Translators Connect ICs Together in Mixed Voltage Systems by Shifting the Logic Levels of the Control and Data Signals

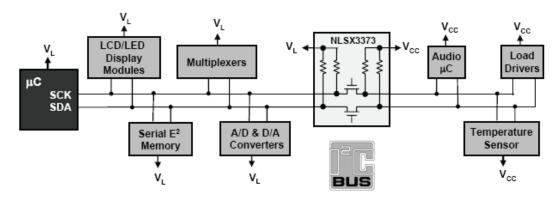


Figure 2. Open-Drain Autosense Voltage Translators Connect a Processor to I<sup>2</sup>C Bus Peripherals that have Different Operating Voltages

The Inter-Integrated Circuit (I<sup>2</sup>C) bus was developed by Philips (NXP) in the early 1980s and has developed into an industry standard protocol. Figure 2 provides a design example of a microprocessor system that incorporates the I<sup>2</sup>C bus. The main advantage of I<sup>2</sup>C is that only two I/O lines are required. A read or write operation is determined by the R/W bit, and microprocessor direction and address pins are not required. In addition, data is received and transmitted independent of the microprocessor's control routine. A read/write operation receives/transmits data to the processor's control routine only after the data buffer is filled. Figure 3 and reference [1] provide details on the  $I^2C$  open-drain bus protocol.

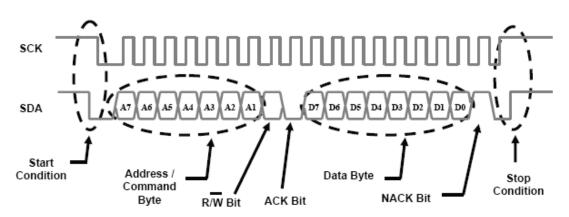


Figure 3. The I<sup>2</sup>C Serial Communication Frame Consists of Serial Clock (SCK) and Serial Data (SDA) Signal Lines

Several popular communication buses have emerged that are similar to  $I^2C$  to serve target applications. The System Management Bus (SMBus), shown in Figure 4, is widely used in PC motherboard applications such as thermal management systems that monitor the microcontroller and PCB temperatures, in addition to controlling the cooling fan. The Power Management Bus (PMBus), shown in Figure 5, is an emerging standard in power delivery systems. In contrast, the  $I^2C$  bus is the preferred bus for general purpose microcontroller applications. The main advantage of the SMBus is the bus recovery feature that resets the open-drain signals if they are at a logic "0" state for more than 35 ms. An overview of the attributes of the  $I^2C$  and SMBus protocols is shown in Table 1.

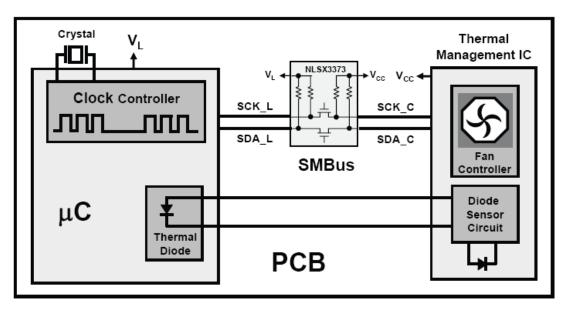


Figure 4. The SMBus is Used to Transfer Control Information and Implement a Clock–Skipping Mode to Reduce the Microcontroller's Temperature

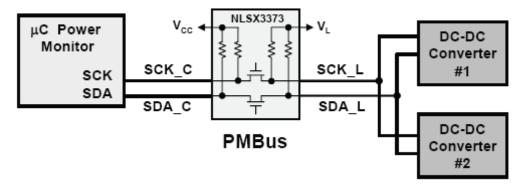


Figure 5. The PMBus is Often Used in Point of Load (POL) Power Supplies to Provide Control and Status Information to a Power Monitor Microcontroller

Parameter	l <sup>2</sup> C	SMBus
Timeout / Data Recovery	No	Yes (35 ms)
Min. Clock Speed	DC	10 KHz
Max. Clock Speed	100 KHz / 400 KHz / 3.4 MHz Standard / Fast / High-Speed Mode	100 KHz
V <sub>H</sub>	0.7 * V <sub>DD</sub> , 3.0 V (Fixed)	2.1 V
VL	0.3 * V <sub>DD</sub> , 1.5 V (Fixed)	0.8 V
I <sub>MAX</sub>	3 mA	350 μΑ

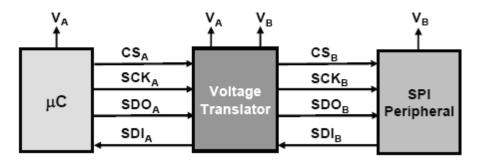


Figure 6. SPI Consists of a Chip Select (CS), System Clock (SCK), Serial Data Output (SDO) and Serial Data Input (SDI) Signals

The Serial Peripheral Interface (SPI) bus, shown in Figure 6, is a synchronous serial communication protocol that can simultaneously receive and transmit data. SPI is a popular protocol developed from the Motorola (Freescale) Master Output Slave Input (MOSI) and Master Input Slave Output (MISO) microprocessor bus. SPI offers a higher data transfer rate than  $I^2C$  because there is no maximum clock frequency specification. A negative feature of SPI is that the protocol requires either a chip select line per peripheral or address decoding.

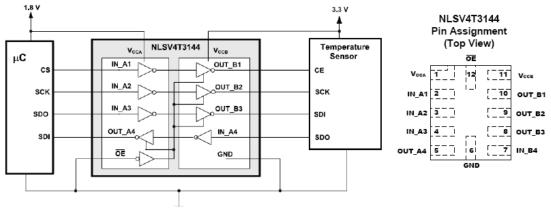


Figure 7. The Three Input / One Output Circuit Topology of the NLSV4T3144 Matches the I/O Structure of the Four Wire SPI Bus

Both uni-directional and autosense voltage translators can be used to interface a microprocessor and SPI peripheral, as shown in Figures 7 and 8. The I/O pin locations of the NLSV4T3144 and NLSX3014 accommodate a straight feed through design, which is a convenient PCB layout feature. Figure 9 shows an autosense translator can be used in SPI ports that use a single bi-directional data line.

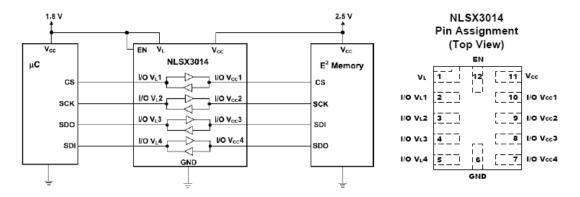


Figure 8. The Autosense Translator's I/O Pins Can Function as Either an Input or Output, Which is an Advantage in SPI Translator Applications

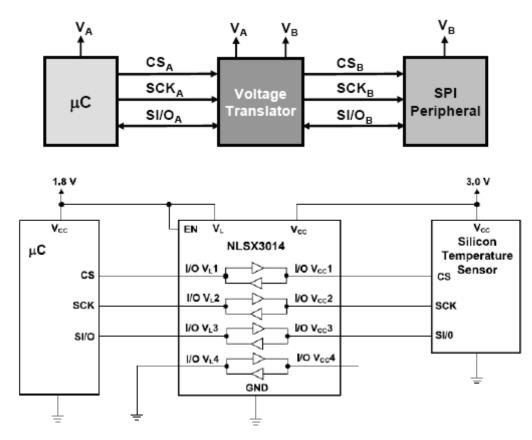


Figure 9. Autosense Translators Can be Used for SPI Ports that Combine the Input (SDI) and Output (SDO) Data Lines into a Single Bi-directional Signal (SI/O)

#### Memory Mapped I/O

Memory Mapped I/O circuits typically use bi-directional with direction pin translators to connect multiple peripheral ICs to a single microcontroller. The directional pin determines if data is received or transmitted to a peripheral IC via a Read/Write statement. The microcontroller address pins select or 'map' multiple peripheral devices to a single data bus. Figures 10 and 11 provide examples of memory map I/O translator applications.

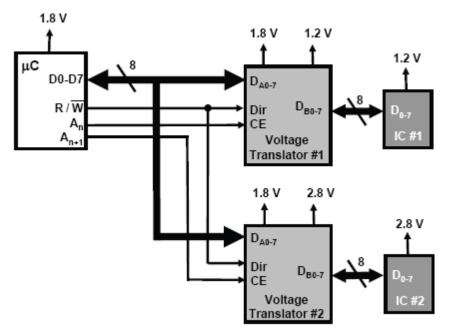


Figure 10. Memory Mapped I/O Translators are Often Used with Relatively High Pin Count Microprocessors that Need Fast Data Transfers

Memory Mapped I/O uses a parallel data format. Therefore the transfer rate is proportional to the number of data bits. In addition, the communication speed is equal to the duration of the Read/Write instruction cycle time of the microcontroller and peripherals; thus, the control program is delayed by slow I/O devices. A disadvantage of Memory Mapped I/O is that address lines are used to generate the chip enables of the peripheral ICs because a relatively large number of microcontroller I/O pins are required. For example, the circuit shown in Figure 10 requires 11 microprocessor I/O lines (8 data, 1 Read/Write, 2 address lines). In contrast, the I<sup>2</sup>C bus uses only 2 I/O lines (SDA, SCK).

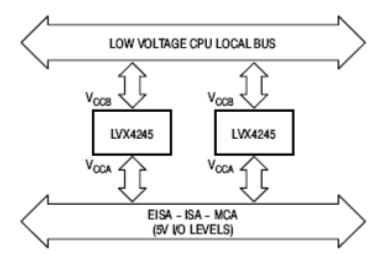


Figure 11. The MC74LVX4245 is a Dual Supply Bi-Directional with Direction Pin Translator that can be Used to Interface a 5 V I/O Bus to a 3.3 V Microprocessor

#### UARTs

A universal, asynchronous receiver / transmitter (UART) communications port can be used to transfer data between the processor and a peripheral device. UART ports are included in most microprocessors and are also available in stand alone ICs. Figure 12 shows a circuit where the UART

transfers data between a control and audio processor. A logic translator is needed in this example because the audio IC operates at a higher voltage than the control processor in order to produce a detectable audio signal. In addition, voltage translators are often required for UARTs in RS-232, RS-422 and RS-485 applications.

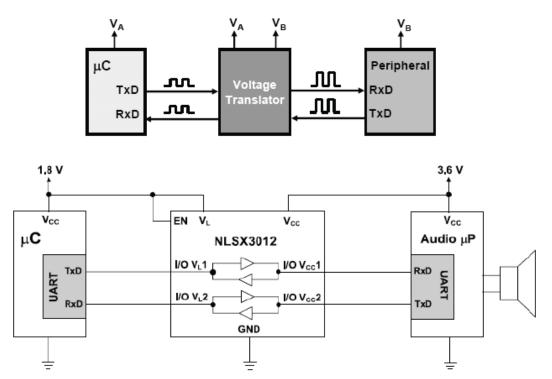
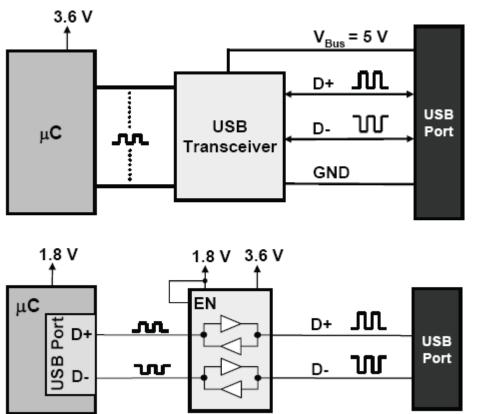


Figure 12. Voltage Translators are Often used with UARTs to Interface a Low Voltage Processor to a Higher Operating Voltage Analog IC, Such as an Audio Processor

#### **USB** Ports

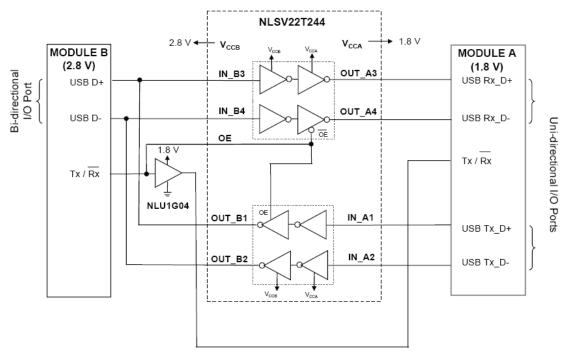
Dual supply voltage translators can be used to shift the voltage levels of a Universal Serial Bus (USB) signal. Figures 13 and 14 provide design examples using an

autosense and uni-directional translator, respectively. Voltage translators offer cost savings over standard USB transceivers.



NLSX3012

Figure 13. An Autosense Translator Can be used to Increase the Voltage of a Low Voltage Microcontroller that has an Integrated USB Port



 $\begin{array}{l} \mathsf{OE} = \mathsf{High}, \, \mathsf{Module B \ Transmits}, \, \mathsf{Module A \ Receives} \\ = \mathsf{B} \to \mathsf{A} \\ \\ \mathsf{OE} = \mathsf{Low}, \, \mathsf{Module \ A \ Transmits}, \, \mathsf{Module \ B \ Receives} \\ = \mathsf{A} \to \mathsf{B} \end{array}$ 

#### Figure 14. A Dual Two Channel Uni-Directional Translator Can Function as a Bi-Directional USB Transceiver

#### Bibliography

 "UM10204: I<sup>2</sup>C Bus Specification and User Manual", NXP Semiconductor, 2007.

#### **Industry Websites for Further Information**

- Power Management Bus (PMBus), <u>www.pmbus.org</u>.
- Systems Management Bus (SMBus), <u>www.smbus.org</u>.

	Autosense Bi-Directional Translators (Push-Pull Output)	Autosense Bi-Directional Translators (Open-Drain Output)
Block Diagram	VL VL VCC VCC VCC VCC VCC VCC VCC VCC VC	V <sub>L</sub> Pretition 10 KΩ N Elics N N Elics N N Elics N N Elics N N Elics N N N N N N N N N N N N N
Attributes	<ul> <li>High Data Rate</li> <li>Low Power Consumption</li> <li>Flexible PCB Design</li> </ul>	<ul><li>High Output Drive</li><li>Low Power Consumption</li><li>Flexible PCB Design</li></ul>
Trade-Offs	Modest Output Current	Modest Bandwidth
Applications	<ul> <li>SPI</li> <li>UARTs</li> <li>USB Ports</li> <li>GPIO</li> </ul>	<ul> <li>I<sup>2</sup>C, SMBus, PMBus</li> <li>SIM / SDIO Cards</li> <li>Display Modules</li> <li>HDMI</li> <li>1-Wire Bus<sup>™</sup></li> <li>GPIO</li> </ul>
ON Products (I/O Channels / Package)	<ul> <li>NLSX3012 (2-bit, UDFN-8)</li> <li>NLSX3014 (4-bit, UQFN-12)</li> <li>NLSX3013 (8-bit, CSP-20)</li> <li>NLSX3018 (8-bit, UDFN-20)</li> <li>NLSX4014 (4-bit, UQFN-12)</li> </ul>	<ul> <li>NLSX3373 (2-bit, UDFN-8)</li> <li>NLSX3378 (4-bit, CSP-12)</li> </ul>

## APPENDIX I: ON DUAL POWER SUPPLY AUTOSENSE VOLTAGE TRANSLATORS

APPENDIX II: ON DUAL POWER SUPPLY UNI-DIRECTIONAL AND BI-DIRECTIONAL WITH DIRECTIONAL PIN
VOLTAGE TRANSLATORS

	Uni-Directional Translators	Bi-Directional with Directional Pin Translators
Block Diagram		$ \begin{array}{c} \overline{OE} \\ \overline{T/R} \\ A1 \\ \hline A2 \\ \hline \hline \\ A2 \\ \hline \\ \hline \\ B2 \end{array} $
Attributes	<ul><li>High Data Rate</li><li>Low Power Consumption</li></ul>	<ul><li>High Data Rate</li><li>High Output Drive</li></ul>
Trade-Offs	Fixed Input & Output Pins	<ul> <li>All I/O Lines Configured for Either A-to-B or B-to-A Single Direction Translation</li> <li>Control Pin Limits Usability in Pin Sensitive Portable Applications</li> </ul>
Applications	<ul><li>SPI</li><li>USB Ports</li><li>GPIO</li></ul>	<ul><li>Memory Mapped I/O</li><li>GPIO</li></ul>
ON Products (I/O Channels / Package)	<ul> <li>NLSV1T34 (1-bit, ULLGA-6)</li> <li>NLSV1T240 / 244 (1-bit, UDFN-6)</li> <li>NLSV2T240 / 244 (2-bit, UDFN-8)</li> <li>NLSV4T240 / 244 (4-bit, UQFN-12)</li> <li>NLSV4T3234 (4-bit, CSP-11)</li> <li>NLSV8T240 / 244 (8-bit, UDFN-20)</li> </ul>	<ul> <li>MC74LVXC4245 (8-bit, SOIC-24, TSSOP-24)</li> <li>MC74LVXC3245 (8-bit, SOIC-24, TSSOP-24)</li> </ul>

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